



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,813	02/24/2004	Jane Lu	2946-D-Z	1174
7590		04/19/2005	EXAMINER	
Jim Zegeer, Esq.		NORRIS, JEREMY C		
Suite 108		ART UNIT		
801 North Pitt Street		PAPER NUMBER		
Alexandria, VA 22314		2841		

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Ak

Office Action Summary

Application No.

10/784,813

Applicant(s)

LU ET AL.

Examiner

Jeremy C. Norris

Art Unit

2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 January 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 11, 12, 15, and 16 rejected under 35 U.S.C. 102(e) as being anticipated by US 6,538,319 (hereafter Terui).

Examiner notes that the phrase “for ball grid integrated circuit packages” is a statement of intended use and thus only requires the ability to so perform. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham, 2 USPQ 2d 1647 (1987)*.

Terui discloses, referring to figure 5, a thermally enhanced printed circuit (PC) wiring board for ball grid integrated circuit packages comprising a relatively thin, conductive metal core layer (31) having oppositely facing surfaces and one or more holes (5) in the metal core at each of a plurality of through-core via sites, a first and second thin rigidifying non-conductive laminate sheet (30) attached to said oppositely facing surfaces, respectively, and at least one conductive circuit pattern (6) on at least

Art Unit: 2841

one of said thin rigidifying non-conductive sheets and a plurality of vias (7) thereon [claim 11], including a plurality of vias (5a) made by plating build-up and connecting to the core from both the top and bottom sides thereof [claim 12], including a plurality of vias selected from Type 1, Type 2, and Type 3 vias as defined by the instant application (see figure 5) [claims 15, 16].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

Art Unit: 2841

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 13, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terui in view of US 5,861,076 (hereafter Adlam).

Regarding claim 13, Terui discloses the claimed invention as described above except Terui does not specifically state that the copper core layer (31, see col. 4, lines 55-65) is in the range of 5-15 mils thick and the organic laminate sheets (see col. 2, lines 30-40) are fiberglass [**claim 13**]. However, it is well known in the art to use 7 mil thick copper foils in printed circuits based on the high conductivity and structural rigidity as evidenced by Adlam (see col. 5, lines 55-65). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use 7 mil thick copper as the core layer in the invention of Terui, as is well known and evidenced by Adlam. The motivation for doing so would have been to use a highly conductive copper foil with sufficient thickness to reduce the chance of the device warping, thus making a more reliable product. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Additionally, it is well known in the art to use fiberglass as an organic substrate in printed circuit board based on the highly dielectric properties and mechanical rigidity as again evidence by Adlam (see col. 5, lines 35-45). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use fiberglass for the laminate sheets in the invention of Terui as is well known in the art and evidenced by Adlam. The motivation

Art Unit: 2841

for doing so would have been to use a known dielectric with high rigidity to reduce the chance of the device warping, thus making a more reliable product. Moreover, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.

In re Leshin, 125 USPQ 416.

In addition, the modified invention of Terui teaches one or more additional non-conductive and conductive layers (6, 8) thereon [**claim 14**].

Moreover, Terui discloses, referring to figure 5, a thermally enhanced printed circuit (PC) wiring board for ball grid integrated circuit packages comprising: a conductive metal core layer (31) having oppositely facing surfaces and one or more holes (5) in the metal core at each of a plurality of through-core via sites, a first and second thin rigidifying non-conductive laminate sheets (30) attached to said oppositely facing surfaces of said conductive metal core layer, respectively, at least one conductive circuit pattern (6) on at least one of said thin rigidifying non-conductive sheets, and a plurality of vias selected from type 1, type 2 or type 3 vias made by plating build-up and connecting to the core selectively from the top and bottom sides thereof, respectively (see figure 5). Terui does not specifically state that the copper core layer (31, see col. 4, lines 55-65) is in the range of 5-15 mils thick and the organic laminate sheets (see col. 2, lines 30-40) are fiberglass [**claim 17**]. However, it is well known in the art to use 7 mil thick copper foils in printed circuits based on the high conductivity and structural rigidity as evidenced by Adlam (see col. 5, lines 55-65). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time

Art Unit: 2841

of invention, to use 7 mil thick copper as the core layer in the invention of Terui, as is well known and evidenced by Adlam. The motivation for doing so would have been to use a highly conductive copper foil with sufficient thickness to reduce the chance of the device warping, thus making a more reliable product. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Additionally, it is well known in the art to use fiberglass as an organic substrate in printed circuit board based on the highly dielectric properties and mechanical rigidity as again evidence by Adlam (see col. 5, lines 35-45). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use fiberglass for the laminate sheets in the invention of Terui as is well known in the art and evidenced by Adlam. The motivation for doing so would have been to use a known dielectric with high rigidity to reduce the chance of the device warping, thus making a more reliable product. Moreover, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Response to Arguments

Applicant's arguments filed 6 January 2005 have been fully considered but they are not persuasive. Applicants allege "Terui is in nowise a printed circuit wiring board for ball grid integrated circuit packages -- it is the "ball grid integrated circuit package" which is attached to applicants' printed circuit wiring board as defined by claims 13 and 14". Firstly, nowhere in Applicants' claims 13 and 14 is there any mention of a "ball grid

Art Unit: 2841

integrated circuit package” attached to the PC board. Thus, Applicants are arguing limitations which are not found in the claims. Secondly, it is readily apparent to one of ordinary skill in the art that printed circuit board is indeed being used “for ball grid integrated circuit packages” as shown in figure 5 and exemplified in col. 2, line 10 – col. 3, line 40. Applicants’ position to the contrary is simply untenable. Finally, it appears to Examiner that Applicants wish to characterize their invention as a board that *receives* a ball grid integrated circuit package. However, it is the Examiner position that the current claim language, given its broadest reasonable interpretation, in no fashion limits Applicants claimed invention to such an embodiment for although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. If Applicants feel this distinction is integral to the invention, language reflecting this narrow interpretation should be added to the claims. Therefore, Applicants’ traversal of the outstanding rejection on these grounds is deemed unsuccessful.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

Art Unit: 2841

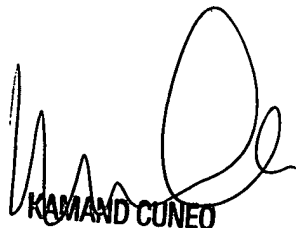
extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN


KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800